REMARKS

A Petition for a Two Month Extension of Time is being filed concurrently herewith. Further, a Submission of Formal Drawings has been filed concurrently herewith including changes to FIGS. 1, 2, 4, 5, 7 and 17. Claims 1-25 are currently pending in the above-identified application. Claims 1-23 have been rejected. Text in two paragraphs has been amended to correct typographical errors. Claim 1 has been amended and new claims 24 and 25 have been added. No new matter has been included in the additional or amended text or in the altered figures. Applicants respectfully request reconsideration in light of the foregoing amendments and following remarks.

The disclosure stands objected to for informalities found on page 19, line 26 and page 27, line 4. Applicants have amended the paragraphs containing the informalities.

Figures 1, 2, 4, 5, 7 and 17 stand objected to for containing various informalities. Applicants have filed concurrently herewith a Submission of Formal Drawings substituting new Figures 1, 2, 4, 5, 7 and 17 correcting the various informalities.

Claims 1-3, 5, 6, 9, 10 and 19-23 stand rejected under 35 U.S.C. §102 as being anticipated by Lepejian. Claim 1 has been amended.

As amended, claim 1 recites a semiconductor inspection system that includes "a navigation system for storing semiconductor chip design information such as CAD data and for setting capturing and inspecting conditions including a region on a semiconductor wafer subject to inspection based on the design information". The semiconductor inspection system further includes "a scanning electron microscope system for performing an inspection by actually capturing the semiconductor wafer in accordance with the

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capturing and inspecting conditions set". Also, "the navigation system sets a template based on the design information, performs a matching process, by using the template, with respect to a pattern within an image provided by the scanning electron microscope system, and re-registers a portion of the image that corresponds to the template as a template". Claims 2, 3, 5, 6, 9, 10 and 19-23 depend upon claim 1.

Lepejian discloses a method for using wafer navigation to reduce testing times of integrated circuit wafers. The disclosure of Lepejian includes the feature of using CAD data in determining whether or not a test should be conducted. Lepejian fails to teach or suggest "perform[ing] a matching process, by using the template, with respect to a pattern within an image provided by the scanning electron microscope system" and "re-register[ing] a portion of the image that corresponds to the template as a template" as recited in claim 1.

Claims 4, 7, 8 and 11-18 stand rejected under 35 U.S.C. §103 as being unpatentable over Lepejian in view of Okubo. Claims 4, 7, 8 and 11-18 depend from claim 1.

As noted above, Lepejian fails to teach or suggest "perform[ing] a matching process, by using the template, with respect to a pattern within an image provided by the scanning electron microscope system" and "re-register[ing] a portion of the image that corresponds to the template as a template" as recited in claim 1. Okubo discloses an electron beam tester. Okubo fails to teach or suggest "re-register[ing] a portion of the image that corresponds to the template as a template" as recited in claim 1.

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New claims 24 and 25 have been added and are believed to be patentable over the cited art.

Applicants believe that each of the presently pending claims are in immediate condition for allowance. Accordingly, the Examiner is respectfully requested to pass this application to issue.

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Respectfully submitted,

By: _(signature)_

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VERSION WITH MARKINGS TO SHOW CHANGES MADE

Text has been amended on pages 19 and 27, claim 1 has been amended, and new claims 24 and 25 have been added.

Replace the paragraph beginning on page 19, line 13:

Fig. 6 is a flowchart of a re-registration process of the SEM image as the template according to the embodiment of the present invention, in the case which the matching processes between the design data and the SEM image are performed in an arbitrary frequency, whereby the SEM image in the position highest in the correlation value among all the correlation values of the SEM images is re-registered as the template. Steps 601 to 604 and Steps 606 to 610 correspond to Steps 201 to 204 and Steps 205 to 209 in Fig. 2, respectively. The matching processes using the design data and the SEM image are iterated by an arbitrary frequency from Step 602 to Step 605, and then in Step 606, the SEM image in the position highest in the correlation value among all the detected positions is re-registered as the template. Accordingly, it is possible to select the SEM image high in the correlation value. When detection is performed a plurality of times. Steps 607 to 609 will be iterated by use of the template. Note that [the] both processes shown in Fig. 4 and in Fig. 6 can be automated by computer programs.

Replace the paragraph beginning on page 27, line 1:

Moreover, in the conventional case of performing the matching process between the design data and the SEM images, it has been impossible to perform a stable matching

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process because the correlation coefficient becomes considerably small due to inadaptability to deformed parts between the design data and the SEM images. In response to the foregoing problem, the present invention performs the matching process to make up the deformed parts by use of the edge information in multiple directions and smoothing thereof in the case that the matching process between the design data and the SEM images takes place. In addition, the present invention performs the matching process between the edge images and the templates of the design data, and performs the matching process after re-registering the part of the SEM image corresponding to the detected position as the template. Therefore, a stable matching process with a high correlation value and a high detection ratio can be achieved.

Amend claim 1:

1. (Amended) A semiconductor inspection system, comprising:

a navigation system for storing semiconductor chip design information such as CAD data [of a semiconductor chip] and for setting capturing and inspecting conditions including a region on a semiconductor wafer subject to inspection based on the design information; and

a scanning electron microscope system for performing an inspection by actually capturing [of] the semiconductor wafer [and for executing inspection] in accordance with the capturing and inspecting conditions [being set up] set;

wherein the navigation system sets a template based on the design information, performs a matching process, by using the template, with respect to a pattern within an

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image provided by the scanning electron microscope system, and re-registers a portion of the image that corresponds to the template as a template.

Add new claims 24 and 25:

24. (New) A semiconductor inspection method by which a pattern within an image provided by a scanning electron microscope is determined by using a template that is registered in advance, the method comprising the steps of:

creating a template based on semiconductor chip design information such as CAD data;

detecting, by a pattern matching process, a position in an image provided by the scanning electron microscope which corresponds to the template; and

re-registering an image portion corresponding to the detected position as a template.

25. (New) A semiconductor inspection comprising:

a navigation system for registering a template used for a matching process for the identification of a portion of a semiconductor wafer subject to inspection; and

a scanning electron microscope system for forming an image based on the irradiation of the semiconductor wafer with an electron beam;

wherein the navigation system sets the template based on semiconductor chip design information such as CAD data, performs a matching process, by using the template, with respect to a pattern within an image provided by the scanning electron microscope

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system, and re-registers as a template a portion of the image that is detected by the

matching process and which corresponds to the template.